CLAIMS

What is claimed is:

1. A multi-giga bit transceiver (MGT) system for converting between parallel data and serial data comprising:

first MGT circuitry for performing a first MGT function;

second MGT circuitry for performing a second MGT function;

at least one regulated power source and at least one unregulated power source, both coupled to selectively provide regulated and unregulated power to the first and second MGT circuitry; and

programmable logic for providing control signals to select and operatively couple the first and second MGT circuitry to one of the at least one regulated and unregulated power sources.

2. The MGT system of claim 1 wherein the at least one regulated power source comprises an unregulated supply and a plurality of power regulators coupled to selectively provide regulated power from the supply to the first and second MGT circuitry.

3. The MGT system of claim 2 wherein the first MGT circuitry comprises a phase-locked loop (PLL).

4. The MGT system of claim 3 wherein the PLL further includes a transmitter phase-locked loop (Tx PLL) for generating a transmitter clock.

5. The MGT system of claim 3 wherein the PLL further includes a receiver phase-locked loop (Rx PLL) for generating a receiver clock.

6. The MGT system of claim 3 further including receiver serial-in-parallel-out circuitry (Rx SIPO).

7. The MGT system of claim 6 wherein the Rx SIPO receives only unregulated power.

8. The MGT system of claim 6 wherein there exists a selectable power regulator for the Rx SIPO circuitry.

9. The MGT system of claim 8 wherein the programmable logic selects between regulated power and unregulated power for the Rx SIPO.

10. The MGT system of claim 2 wherein there exists a selectable power regulator for a first MGT circuit group that includes a Tx PLL and a Rx PLL that are jointly coupled to one of the regulated power source and the unregulated power source.

11. The MGT system of claim 2 wherein the power regulators each further comprises a current mirror having a reference current stage and selectable current mirror stages for providing one of a plurality of current levels into an output node.

12. The MGT system of claim 11 wherein the power regulators of the plurality of selectable power regulators each further comprises a voltage regulator stage for adjustably sinking current from the output node to maintain a specified output voltage at the output node.

13. The MGT system of claim 12 wherein the voltage regulator stage further includes an amplifier and a voltage divider with selectable divider resistors to create selectable voltage divider ratios, the voltage divider coupled to an input of the amplifier.

14. The MGT system of claim 13 further including logic for selecting the selectable divider resistors wherein the

voltage regulator stage is further coupled to receive a reference voltage and wherein the logic selects the selectable divider resistors responsive to fluctuations in the reference voltage from an expected value to create a specified voltage divider ratio to enable the voltage regulator stage to produce an expected output voltage.

15. A power regulator within programmable logic device (PLD) coupled to a power supply comprising:

a current mirror having a reference current stage and selectable current mirror stages for providing one of a plurality of current levels into an output node;

a voltage regulator stage coupled to adjustably sink current from and source current to the output node to maintain a specified output voltage at the output node; and

wherein the output node of the current mirror is further coupled to at least one selectable switch to selectively provide regulated power to at least one of a Tx PISO, a Tx PLL and an Rx PLL.

16. The power regulator of claim 15 wherein the at least one selectable switch also selectively provides regulated power to an Rx SIPO.

17. The power regulator of claim 15 wherein the voltage regulator stage further includes an amplifier and a voltage divider with selectable divider resistors to create selectable voltage divider ratios, the voltage divider coupled to an input of the amplifier.

18. The power regulator of claim 17 wherein the voltage regulator stage is further coupled to receive a reference voltage from a reference circuit and control signals from logic within the PLD for selecting divider resistors to create a specified voltage divider ratio to compensate for variations in the reference voltage.

19. A method within a high data rate transceiver for converting between parallel data and serial data and for providing regulated power and unregulated power, comprising:

generating a transmitter clock and a receiver clock;

converting parallel data into serial data according to the transmitter clock;

converting serial data into parallel data according to the receiver clock;

selectively providing regulated and unregulated power to circuitry for generating the transmitter and receiver clocks and to circuitry for converting the parallel data into serial data; and

selecting between regulated power and unregulated power and generating corresponding control signals to circuitry for generating the transmitter and receiver clocks and circuitry for converting the parallel data into serial data.

20. The method of claim 19 further including selectively providing regulated power and unregulated power to an Rx SIPO.

21. The method of claim 20 further including selecting and providing one of a plurality of current levels into an output node.

22. The method of claim 21 further including adjustably sinking current from the output node to maintain a specified output voltage at the output node.

23. The method of claim 21 further including selecting and adjusting voltage divider ratios coupled to an input of a voltage regulator that performs the step of adjustably sinking current from the output node to maintain the specified output voltage at the output node.